What is claimed is:

1. A semiconductor device provided with a temperature detection circuit for measuring a temperature of a CPU which is provided in a chip same as a chip on which the CPU is mounted.

2. The semiconductor device according to Claim 1, wherein the temperature detection circuit detects a temperature using a temperature dependency of off leak currents of transistors.

3. The semiconductor device according to Claim 2, wherein the temperature detection circuit comprises a temperature detection part for increasing a potential of a live node connected to a stray capacitance by charging the stray capacitance of transistors with the off leak currents, and for detecting that a temperature of the CPU reaches a given temperature by comparing a potential level of the live node with a threshold value of the transistor, and a detection signal output part for outputting and holding a detection signal which is driven by a signal issued by the temperature detection part.

4. The semiconductor device according to Claim 3, wherein the temperature detection part comprises a first PMOS transistor and a first NMOS transistor connected in series between a power supply potential VDD and a grounding potential, and the live node is a junction between a drain of the first PMOS transistor and a drain of the first NMOS transistor, and the stray capacitance between the live node and the grounding potential is charged with a current differential between the off leak current of the first PMOS transistor and the off leak current of the first NMOS transistor when the first PMOS transistor and the first NMOS transistor are in OFF state.

5. The semiconductor device according to Claim 3, wherein the detection signal output part comprises a second PMOS transistor connected between the power supply potential VDD and the grounding potential, a series circuit comprised of second and third NMOS transistors connected in series to each other, and a data holding circuit connected to an output node of the series circuit, wherein a drain of the second PMOS transistor is connected to the output node and a drain of the second NMOS transistor while a gate of the second NMOS transistor is connected to a gate of the first PMOS transistor and a drain thereof is connected to a drain of the third NMOS transistor, and a gate of the third NMOS transistor is connected to the live node, and a source thereof is grounded, and wherein the output node is pre-charged by the second PMOS transistor when starting the detection of the temperature, and the second and third NMOS

transistors are rendered in ON state when a potential of the live node exceeds a threshold value of the third NMOS transistor, so that the pre-charged electric charge accumulated in the output node is discharged to change the potential of the output node and the changed potential is hkept in the data holding circuit.

6. The semiconductor device according to Claim 5, wherein the detection signal output part further comprises a third PMOS transistor connected to the power supply potential VDD at its source, to the output node at its gate, and to the live node at its drain, and wherein said third PMOS transistor is rendered in ON state when the temperature of the CPU reaches a set temperature, and the pre-charged electric charge of the output node is discharged to accelerate the charging of the stray capacitance of the live node.